IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 09/541,732, filed April 3, 2000, now U.S. Patent 6,732,223, issued May 4, 2004.

Please amend paragraph **[0024]** as follows:

[0024] FIG. 1 depicts an embodiment of the present invention comprising a ~~portion~~ circuit 2 of a memory bank control logic circuit for use with dynamic random access memory ("DRAM"). The circuit ~~portion~~ 2 of the first embodiment includes both write and read counters 4 and 6 (also called pointers), write and read address decoders 8 and 10, FIFO buffers 12, and column and row address output circuits 14 and 16. In a typical FIFO buffer system, an "empty" flag signal indicates whether valid data is contained in a FIFO buffer 12. When a valid write operation occurs, the "empty" flag is replaced by a "full" flag. If a read operation occurs when the read pointer is pointing to the same address as the write pointer, then the empty part will be read, resulting in a delay due to reading an empty buffer. This also moves the read counter forward one whether or not there is any data to be read.

Please amend paragraph **[0027]** as follows:

[0027] FIG. 2 is a schematic diagram of a write counter 4 for use with an embodiment of the invention. The write counter 4 includes two registers 18 and 20 and outputs the current counter setting. After receiving a reset signal through the reset terminal or input 22, both of the registers 18 and 20 have a low output. When the write latch signal fires through the write latch terminal or input 24, the current counter setting signal will indicate a first address having two digits output in serial order. Each time the write latch signal fires through the write latch terminal or input 24, the two registers 18 and 20 will increment the two digit binary address by one until the highest address is reached. For a system with outputs from $n = 2$ registers, the highest address is $2^n-1 = 3$. The following is a table of the incremental outputs for each of the registers 18 and 20 of the write counter 4:

First Register 18	Second Register 20
0	0
1	0
1	1
0	1

Please amend paragraph **[0028]** as follows:

[0028] FIG. 3 is a schematic diagram of a read counter 6 for use with an embodiment of the invention. Like the write counter 4 of FIG. 2, the read counter 6 of FIG. 3 includes two registers 26 and 28, the serial outputs of which indicate the current counter setting. However, unlike the write counter 4, the read counter 6 also includes a third register 30, the output of which, in combination with the output of the second register 28, indicates the previous counter setting of the read counter 6. Thus, after receiving a reset signal through the reset terminal or input 22, all three of the registers 26, 28 and 30 have a low output. When the read latch signal fires through the read latch terminal ~~24~~ or input 32 to determine whether or not there is data stored in the memory buffer, the current counter setting signal will indicate a first FIFO buffer address having two digits output in serial order. The previous counter setting signal will similarly indicate a buffer address, but because the second and third registers 28 and 30 will not have incremented yet, the second and third registers will indicate the previous counter setting, both having a low output. Each time the read latch signal fires through the read latch terminal or input 32, the content of the first register 26 will transfer to the second register 28, and the content of the second register will transfer to the third register 30. Thus, the serial combination of the output of the second register 28, which is found as the second bit in the serial output of the current counter setting, with the output of the third register 30, which is the previous counter setting signal, is always one transfer behind the serial combination of the outputs of first register 26 and the second register 28. The following is a table of the incremental outputs for the registers of the read counter:

First Register 26	Second Register 28	Third Register 30
0	0	0
1	0	0
1	1	0
0	1	1
0	0	1

Please amend paragraph **[0032]** as follows:

[0032] In operation, after the reset signal fires through reset terminal or input 22, each of the registers 18, 20, 26, 28 and 30 in both the write and read counters 4 and 6, also called pointers, are targeted at address 0. Being targeted at address 0 means they are currently set to read from and write to both the column and row FIFO buffers 0 46 and 48. A write latch signal through write latch terminal or input 24 and a read latch signal through read latch terminal or input 32 are each respectively used to toggle the write counter (or write address pointer) 4 and read counter (or read address pointer) 6. At some time after the first address is latched into FIFO buffers 0 46 and 48, the read latch signal may be asserted to read out the oldest data in the FIFO buffer circuit, for this case, namely the first address latched into FIFO buffers 0 46 and 48. On the first read latch signal, the first and second registers 26 and 28 of the read counter 6 increment by one counter setting to point at the FIFO buffers 1 50 and 52. However, the serial combination of the outputs from the second and third registers 28 and 30, which indicates the previous counter setting rather than the current counter setting, still points at the FIFO buffers 0 46 and 48. Because the read address decoder 10 takes as its input the output from the third register 30 and combines it in serial order with the output from the second register 28, the read counter/decoder combination has, in essence, ignored the first read latch signal. Thus, even after the first read latch signal, the read counter 6 is still pointing to the first FIFO buffers 0 46 and 48. Each successive firing of the read latch signal through read latch terminal or input 32 will move the read address pointer sequentially ahead one FIFO buffer register. This automatically causes a

minimum of one buffer position offset between the read and write pointers. The result of this operation is, while a register is being read, other registers can be loaded since the write pointer is at least one position ahead of the read pointer. There is an assumption, however, that to maintain this relationship, every read pointer change requires at least one preceding write pointer change. It will be obvious to one of skill in the art how to program the logic controlling this circuit to maintain this relationship.

Please amend paragraph **[0033]** as follows:

[0033] The write and read address decoders 8 and 10 are conventional 2 to 4 decoders, meaning that they take a binary input of two bits and translate it into a signal on one of four outputs corresponding to the value of the two bit binary input. Write signals 40 output from the write address decoder 8 are Write_<0>, Write_<1>, Write_<2> and Write_<3>. Each of these signals as well as its inverse, created by inverters 44, is fed to two of the FIFO buffers 12 corresponding to the number within the ~~brackets <>~~ brackets < > following the signal type. For example, the Write_<0> and Write <0> signals are fed to each of the FIFO buffers 0 46 and 48. Similarly, the Read signals 42 output from the read address decoder 10, Read_<0>, Read_<1>, Read_<2> and Read_<3>, along with their inverse, are each fed to two of the FIFO buffers 12 corresponding to the number within the ~~brackets <>~~ brackets < > following the signal type. Thus, Read_<1> and Read <1> are both fed to each of the FIFO buffers 1 50 and 52.

Please amend paragraph **[0037]** as follows:

[0037] FIG. 8 is a block diagram of an electronic system 70 which includes DRAM 72 comprising the register/FIFO circuit 2 as shown in FIG. 1. ~~Either~~ Any of the specific preferred embodiments as shown in FIGS. 1-6, or many other specific embodiments not shown herein but which accomplish similar designs, may also be used. The electronic system 70 includes a processor 74 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. Additionally, the electronic system 70 includes one or more input devices 76, such as a keyboard or a mouse, coupled to the processor 74 to allow an

operator to interface with the electronic system 70. Typically, the electronic system 70 also includes one or more output devices 78 coupled to the processor 74, such output devices typically being a printer, a video terminal or a network connection. One or more data storage devices 80 are also typically coupled to the processor 74 to store data or retrieve data from external storage media (not shown). Examples of typical storage devices 80 include magnetic hard and floppy disks, tape cassettes, and writeable compact disks (CDs). The processor 74 is also typically coupled to a cache memory 82, which is usually static random access memory ("SDRAM"), and to the DRAM 72. It will be understood, however, that the register/FIFO circuit 2 may also be incorporated into any one of the input, output and storage devices 76, 78 and 80.